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A UNIVERSAL FRONT-END STAGE FOR ELECTROPHYSIOLOGICAL MAPPINGS

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Abstract-**This paper describes a front-end stage that has been implemented and embedded into instruments dedicated to a wide variety of electrophysiological mapping applications. Emphasis during the design phase has been put towards flexibility, simplicity, and performance in various environments.**

Keywords **– Electrophysiological recordings, amplifier, switches, noises, bias current, offset, impedance, CMMR, drifts.**

I. Introduction

The analog input portion of a signal conditioning stage embedded in any electrophysiological (EP) recording systems is very critical. The main reason is that it is the only part of the system directly dependent upon the characteristics of an external device or electrode. Furthermore, to maintain maximum SNR, a high amplification at the input is likely to be used such that any distortions, offsets, and/or errors introduced prior to such amplification will be translated into significant errors and impose severe limitations. For a universal front-end circuit, the problem becomes more tedious since the characteristics of such external device or electrode are unknown as well as the applications and hence, the electrophysiological signal characteristics as well. In this paper, we shortly describe such universal front-end signal conditioning circuit. Although many alternatives exist, the circuit presented here is a first attempt using adequate tradeoffs to offer sufficient performance for a wide range of EP applications.

II. Circuit Architecture

The diagram of the proposed front-end stage is shown in Fig. 1.

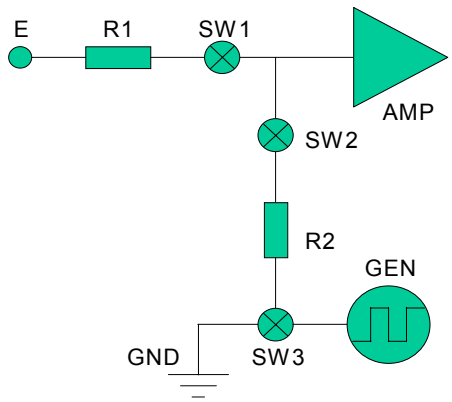

Fig. 1. Simple diagram of the universal front-end stage used to support a variety of electrophysiological mappings (only one of the two terminals is shown for simplicity).

In the diagram, an unknown electrode "E" is connected to the input of an amplifier "AMP" through a resistor "R1" and a switch "SW1". The input of the same amplifier can also be connected to the analog ground "GND" or to an external signal generator "GEN" through "SW2", "SW3", and "R2".

The input stage is controlled by the SPST-switches "SW1" and "SW2" with one SPDT-switch "SW3", connecting "R2" to either "GND" or "GEN".

III. Modes of Operation

Table 1 shows the settings of the switches in the main modes of operation.

TABLE I
SWITCHING MODES

Operation	SW1	SW2	SW3
Recording	ON	OFF	N/A
Calibration	OFF	ON	GEN
Auto-zeroing	OFF	ON	GND
Checking Electrode	ON	ON	GEN
Impedance Tomography	ON	ON	GEN
Stimulation	ON	ON	GEN
Signal Attenuation	ON	ON	GND
Isolation	OFF	ON	GND
Single-ended - Isolated	OFF	ON	GND
Single-ended - Non-isolated	ON	ON	GND

In Table 1, an "ON" state means that the switch is closed. During recording, by selecting "AMP" with significantly high input impedance "Z", "R1" would have no real effect. Furthermore, a high-Z will minimize loading error, especially with high electrode impedance. Another concern is a degradation of DC performance by the additional input offset generated by the amplifier's bias current "I_B" flowing though ($E + R1 + R_{SW1}$) where R_{SW1} is the "Ron" (ON resistance) value of "SW1". With signal amplitudes as low as a few microvolts (respective to "GND") and a +FSR of 5V, a high amplification at the input is highly desirable. Neglecting offset errors and considering only "$I_B = 10$ nA" as in several good instrumentation amplifiers and a gain of "G = 500" at the first amplification stage, we are already limited to "max E $\approx$ 1MΩ". Microelectrodes are becoming very popular in several studies and knowing that they are characterized with impedance in the order of several Mohms, making "I_B" small enough is already becoming a real priority in the development of a universal front-end stage. We have selected the INA110 [1], a monolithic FET input instrumentation amplifier with a "max $I_B = 50$ pA" or "max $I_B = 100$ pA" for the SOIC and the DIP package respectively. Despite the slightly higher bias current, the DIP version has been selected to allow the user to change the INA110 by the pin-compatible AD624 [2] offering slightly lower input noises at the expense of a "max $I_B = 15$ nA" for the best version available. When checking the electrode's contact impedance, at least one more

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Abstract

Subject Terms

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channel must be configured in recording mode. For checking or characterizing the electrodes including electrodes' contact, during impedance tomography, or during stimulation, a current "I" is injected from "GEN". The high input differential impedance ($Z_{IN} \approx 5 \times 10^{12}\ \Omega \parallel 6$ pF) of the INA110 forces "I" to flow towards "E" through "R1", "R2", and the sum of "Ron" from "SW1" to "SW3", provided that the output impedance of "GEN" is sufficiently high. When measuring large signals such as defibrillation shocks, the input signal must be attenuated. In Fig. 1, such first stage's attenuation factor is given by $\{(R2 + R_{SW2} + R_{SW3}) \bullet (R1 + R2 + R_{SW1} + R_{SW2} + R_{SW3})^{-1}\} \bullet G$. Because the variation in "Ron" for FET switches can be significant (in the order of 15 ohms in the best case), accuracy in the attenuation factor can be significantly affected. Because of that and other factors mentioned later, relays have been chosen to implement the switches. Because relays have no Ron, the expression of the first stage attenuation factor can be reduced to $\{R2 \bullet (R1 + R2)^{-1}\} \bullet G$.

The isolation mode is typically used to protect the system against large electrostatic discharges when no measurement is being performed, to protect the system during measurement against excessively large voltages or currents such as defibrillation shocks exceeding the safe operating attenuation mode, and to perform system calibration. Since in all isolation modes, the respective amplifier's inputs are completely disconnected from "E", a bias current path is provided through "SW2" and "SW3" to avoid channel saturation or excessive drift by charging stray capacitance.

IV. Components

A. Resistors

By default, both "R1' and "R2" are low price metal-film high-precision (1%) resistors with good temperature coefficient. One-percent metal-film resistors are often selected instead of carbon-film resistors for applications requiring excellent accuracy and stability. Because the specified 1% margin of the rated value can be exceeded due to temperature change, operation at full rate, and high humidity, all these factors must be controlled adequately. Another factor to consider is the drift with time, which can also increase the error by a factor of approximately 0.5%. The PCB for the front-end stage can also accommodate wire-round resistors for applications requiring exceptionally accurate and stable performance.

The values of "R1" and "R2" were selected to provide a maximum attenuation factor of 500 such that input voltage exceeding 2 kV could be measured. Furthermore, the value of "R1" was selected such that it would not contribute to increase the input noise level by ensuring that the thermal resistance noise (Johnson noise) "E_R" would not exceed the amplifier's noise "E_A". Since both error sources are independent and random, the rms input noise "E_{IN}" can be estimated as $E_{IN} = [(E_R)^2 + (E_A)^2)]^{1/2}$ with $E_R = (4kTB \bullet R1)^{1/2}$ where k is the Boltzman's constant (1.381×10^{-23} J/°K); T is the temperature in Kelvin (°C + 273.2°); B is the effective bandwidth in hertz; and $E_A = [(E_{AIN})^2 + (E_{AOUT} / G)^2)]^{1/2}$ where E_{AIN} and E_{AOUT} are the amplifier's input and output noises respectively. Since the Power Spectral Density (PSD) of thermal noise is white, i.e. it does not vary with frequency, the spectral density is often expressed in units of $V/(Hz)^{1/2}$. Hence, it can be easily deduced that $R1 \le (E_A \bullet (4kT)^{-1/2})^2$. From [1], because we have a best case $E_A \approx 10$ $nV/(Hz)^{1/2}$ up to 10 kHz (most EP applications operate within DC and 10 kHz bandwidth), we have at room temperature $R1 \le 6$ kΩ. The next lower standard value easily found commercially of R1 = 5.1 kΩ combined with R2 = 10.2 Ω (1% tolerance) have been selected, providing an attenuation factor of 501. Notice that the lowest standard values for R2 available commercially are 10.0, 10.2, and 10.5 providing attenuation factors of 510, 501, and 485 respectively. With the above configuration, the noise remains at a minimum level unless the electrode's source impedance becomes larger than 6 kΩ. For instance, E_{IN} with a source impedance of 1 MΩ will already exceed 100 $nV/(Hz)^{1/2}$. Since the current noise density $I_n = 1.8$ $fA/(Hz)^{1/2}$, it will only exceed the 10 $nV/(Hz)^{1/2}$ with source impedance exceeding 5.5 MΩ. The value of "R2" had also to be relatively small in order to have software programmable differential or single-ended selection without the need for extra components at the front-end stage. For instance, in single-ended recording (Table 1), one of the two amplifier's terminals would be connected to "GND" through "SW2", "SW3", and "R2". In our implementation (assuming "SW1" to be in the OFF state), a maximum additional input offset error as low as 1 nV created by "$R2 \bullet I_B$" would appear in the terminal connected to ground when performing single-ended recording.

With a maximum expected input voltage of 2 kV when in attenuation mode (Table 1), "R1" was selected with a power rating of 1 Watt (33 Joules for 30ms defibrillation shock duration appearing at "R1" terminals). Although some modern defibrillators can deliver shocks in excess of 300 Joules, such power rating should be adequate since it is unlikely that in a worst case with 2 kV potential appearing at "R2" terminals, more than 500 µA will flow through each lead. Considering the voltage divider effect created by "R1" and "R2", a maximum of 4 V would appear at the amplifier and "R2" terminals. Therefore, "R2" was selected with a power rating of 1/4 W to provide for wide safety margin without imposing significant increase in the size of the package.

B. Switches

A switch can be categorized as either mechanical or electronic. Because the modes of operation listed in Table 1 must be under computer control, mechanical DIP-switches requiring manual interventions were not considered for the universal front-end stage. The switching time of electronic switches including the popular LC^{2}MOS precision quad switches such as the ADG411 [3] are typically much faster than computer controlled mechanical switches such as relays (nanosecond versus millisecond range) but have ON

resistance, leakage current, and charge injection problem due to channel gate capacitance. For instance, one of the best electronic switch, the JFET 2N4391 [4] has a maximum drain-source Ron of 30 Ω with 15 Ω tolerance and gate leakage current of approximately 1 nA which is much greater than the 100 pA bias current of the amplifier. Furthermore, leakage gets worse at elevated temperature and tends to double for every 10 ^{o}C increase in temperature. The error introduced by Ron in the attenuation mode for instance could have been made less significant by increasing both "R1" and "R2" values at the expense of increasing significantly the input noises level and the input offset error during single-ended recording. Furthermore, electronic switches typically lack OFF isolation (60 dB for the ADG411, 412) and several characteristics of PMOS and CMOS switches change with frequency and/or signal amplitudes causing significant non-linearity and distortions although JFET switches are much better in this respect. Analog switches unlike relays also have characteristics that change with temperature and lack galvanic isolation. Just the excessive leakage current inherent in electronic switches alone forced us to use relays despite the larger physical size, the lower switching frequency, and higher power dissipation which were considered to be less critical in this particular design.

C. Amplifier

A monolithic amplifier has the advantages of low cost and known characteristics. FET amplifiers such as JFET have extremely low "I_B" and current noise (good noise performance with large source impedance) but with much larger offset voltage and drift with temperature. Although the offset can be trimmed, fluctuations in temperature must be minimized when working with a FET amplifier like the INA110 used in our particular implementation. MOSFET amplifiers have a lower "I_B" compared with FET amplifiers but also show excessive and non-convenient offset drift with time compared with bipolar and JFET amplifiers. Furthermore, the lower "I_B" obtained with MOSFET is unnecessary in our case. Bipolar amplifiers were not considered because of the excessively large "I_B" despite the low input voltage offset, drift, and voltage noise.

Unlike bipolar-transistor input amplifiers where the input current, being the base current, decreases with an increase in temperature, FET-input amplifiers like the INA110 where "I_B" is actually the gate leakage current will increase with an increase in temperature. For the INA110, "I_B" is likely to increase by a factor of approximately 10 for a 30 ^{o}C rise above room temperature. For an excessive 65 ^{o}C, "I_B" may reach a maximum value of 1 nA which combined with a worst case 5 MΩ source impedance will produce a 2.5 V output offset with G = 500. This is still acceptable even with a worst case amplifier's offset current of 50 pA considering that recorded signals' amplitudes are likely to be less than 5 mV.

The RTI offset voltage of an instrumentation amplifier is typically expressed as $V_{FST} = \pm (V_{FSTIN} + V_{FSTOUT} / G)$ where V_{FSTIN} and V_{FSTOUT} are the input offset and output offset voltages respectively with maximum values of 500 and 5000 μV respectively for the INA110AG. At low gains, only adjustment of the output offset is typically required whereas for G > 100 as typically used in EP recordings, the input offset becomes more important although both input and output offsets can be corrected for optimal results. However, correcting for offsets will add drift by approximately 0.33 μV/^{o}C per 100 μV adjustment in input offset voltage which will add to the initial maximum drift of ± (5 + 100/G) μV/^{o}C of the INA110AG. To minimize sensitivity to variation in temperature and because manual adjustment may not be practical especially with systems relying on a large number of recording channels, the present implementation does not provide on-board analog offset corrections but provides all the connections necessary to add external offset adjustment circuits. By default, the front-end is designed for systems using auto-zeroing techniques, where neither offset or offset drift, are of concern. The only drawback is a decrease in the available FSR. Nonetheless, considering the low bias current, maximum source impedance, and the small EP signal amplitudes, channel saturation is unlikely to occur except in extremely bad conditions and/or with excessive baseline drifts. Nevertheless for overload recovery, a 1 μs typical would be required for the amplifier's output to return to linear operation following the removal of a 50% input overdrive voltage. Auto-zeroing is performed as shown in Table 1 where one terminal is connected as depicted in the auto-zeroing set-up and the other terminal from the same amplifier is connected for calibration (Table 1) with "GEN" providing a very accurate DC reference voltage V_{REF}.

Internal amplifier's laser trimmed gain set resistors guarantee high gain accuracy and low gain drift with guaranteed values and maximum gain errors of 1 (0.02%), 10 (0.05%), 100 (0.1%), 200 (0.2%), and 500 (0.5%) with maximum gain temperature coefficients ranging from ± 10 to ± 50 ppm/ ^{o}C and maximum non-linearity ranging from ± 0.005% to ± 0.02% of FS (twice these error values for the AG series). By combining the resistors, we can obtain additional gain values with typical accuracy of 300 (0.25%), 600 (0.25%), 700 (2%), and 800 (2%). Additional gain values could have been implemented with external resistors including amplification at the second amplifier's stage using H pad attenuator but it would have been very difficult to maintain good accuracy and adequate gain drift. Furthermore, we felt that the gain values listed above provided an adequate choice and additional values were unnecessary. Again, relays where selected as software controlled gain switches because of the zero ohm contact and insensibility to variation in temperature. The Ron of analog switches would decrease the maximum gain achievable and furthermore, decrease substantially the gain accuracy while increasing the drift and non-linearity. Gain and offset calibrations are performed simultaneously with the same procedure explained earlier for calibration and auto-zeroing.

The high-bandwidth INA110 has excellent dynamic performance for EP applications. The gain-bandwidth

product defines the available gain of the amplifier for a given bandwidth. As a rule of thumb, the amplifier's bandwidth (assuming a sine wave input) should be greater than 100 • G • f_{max} where f_{max} = 10 kHz is the typical maximum frequency chosen to support most EP recordings. With G = 500 we need a minimum amplifier's unity-gain bandwidth of 500 MHz. The peak-peak output voltage of the amplifier is given by "$V_{P-P} \leq S/\pi f_{max}$" where S is the amplifier's slew rate. With a specified worst case S = 12 V/µs with V_{P-P} = 10 Volts, we have f_{max} = 380 kHz > 10 kHz (can be slightly decreased by the additional capacitance of the optional low profile and low capacitance socket used to install the amplifier). Although high bandwidth amplifiers may prove useful in several EP applications, the drawback is that high frequency noises are more susceptible to pass through the amplifiers with less attenuation than a low bandwidth amplifier. Therefore, proper techniques to minimize noise coupling at the inputs are very critical, especially with high-Z amplifiers. To help eliminating coupling noises, the amplifiers is characterized with a minimum of 100 dB (G ≥ 100 ≤ 1 kHz) CMRR (90 dB at 10 kHz with G = 500) with a source imbalance of 1 kΩ < 100 Ω maximum error between R1's in amplifier's terminal pair (106 dB if not AG series). Although the board allows the implementation for AC coupling, it would be unnecessary in most cases and should be avoided because it will likely decrease significantly the CMRR. With the rare occurrence of excessive baseline drift, a bootstrapped AC coupling configuration [5] where the CMRR is maintained high can also be implemented. The implementation of the universal front-end stage is shown in Fig. 2.

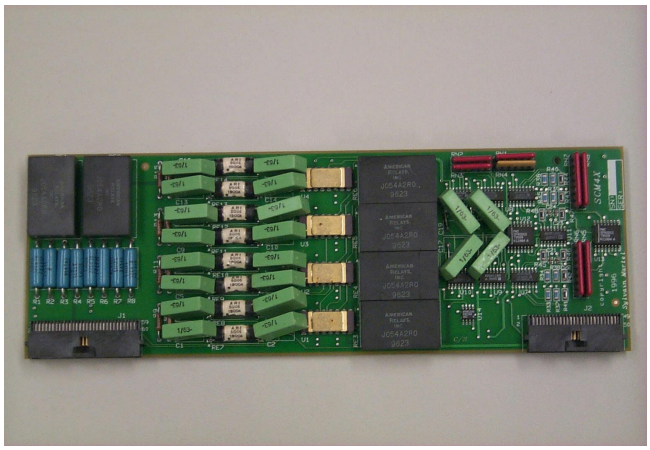

Fig. 2. Photograph of the front-end module.

V. Conclusion

The main design issues and tradeoffs for a universal front-end stage dedicated to EP studies have been described briefly. It was shown that it is not an easy task but it is possible with current off-the-shelf parts to build a front amplification stage that will behave adequately for most applications and tasks for recording EP signals.

References

[1] "INA110". Data Sheet**,** Burr Brown, 1989.
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[5] US Patent 5,300,896